REMARKS

After entry of this amendment, claims 1-71 remain pending. In the present Office Action, claims 1-4, 11-24, 31-36, and 43-49 were rejected under 35 U.S.C. § 102(b) as being anticipated by James L. Turley's Advanced 80836 Programming Techniques ("Turley"). Claims 5-10, 25-30, and 37-42 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Turley in view of Van Dyke et al., U.S. Patent No. 6,418,524 ("Van Dyke"). Applicants respectfully traverse these rejections and request reconsideration.

Rejections Fail to Meet the Requirements of 37 C.F.R. § 1.104(c)(2)

Applicants respectfully submit that the rejections in the present Office Action fail to meet the requirements of 37 C.F.R. § 1.104(c)(2), which states: "When a reference is complex or shows or describes inventions other than that claimed by applicant, the particular part relied on **must** be designated **as nearly as practicable**. The pertinence of each reference, if not apparent, **must** be **clearly explained** and each rejected claim clearly specified". Applicants respectfully submit that the portion of Turley cited in the present Office Action is not designated as nearly as practicable and the alleged pertinence of Turley is not clearly explained.

With few exceptions, the present Office Action rejects all of the claims with reference to the same 33 pages of Turley, without any comment or any attempt to highlight features from these pages that are alleged to correspond to claimed features. Given the length of the citation and the numerous features of the 80386 processor described in the citation, the rejections fail to designate the part relied on as nearly as practicable. Furthermore, given the lack of any comment describing what in Turley is alleged to correspond to various claim features, the rejections fail to clearly explain the alleged relevance of Turley to the claims. **Applicants respectfully request that either the Examiner withdraw the rejection or specifically point out the teachings of Turley that are alleged to correspond to each of the claim features** with the specificity required by the above highlighted rules. Applicants submit that the present Office Action is so vague as to the alleged rejections that a subsequent action meeting the

requirements of the above rules with regard to the Turley citations would constitute a new grounds of rejection and thus should not be made final given that the independent claims have not been amended in this amendment.

Claims 1-43

Applicants respectfully submit that each of claims 1-43 recites a combination of features not taught or suggested in Turley, nor Turley in view of Van Dyke. For example, claim 1 recites a combination of features including: "a third storage location configured to store a mode indication, the mode indication indicative of whether or not a first mode defined in the processor architecture is active; and a processor configured to generate the mode indication responsive to the first indication and the second indication". While the specific teachings of Turley that are alleged to correspond to the above highlighted features are unclear (see the discussion above), Applicants can find no teaching in the cited section of Turley that teaches or suggests the above highlighted features.

For at least the above highlighted reasons, Applicants submit that rejection of claim 1 is unsupported in the art and should be withdrawn. Claims 2-20 depend from claim 1, and thus the rejection of these claims is also unsupported in the art for at least the above highlighted reasons. Each of claims 2-20 recite additional combinations of features not taught or suggested in the cited art.

Claim 21 recites a combination of features including: "a circuit coupled to the first register and the second register, wherein the circuit is configured to generate a mode indication responsive to the first indication and the second indication, wherein the mode indication is indicative of whether or not a first mode defined in a processor architecture of the processor is active, and wherein the circuit is configured to store the mode indication in a location addressable by an instruction". While the specific teachings of Turley that are alleged to correspond to the above highlighted features are unclear (see the discussion above), Applicants can find no teaching in the cited section of Turley that teaches or suggests the above highlighted features.

For at least the above highlighted reasons, Applicants submit that rejection of claim 21 is unsupported in the art and should be withdrawn. Claims 22-32 and 63-65 depend from claim 21, and thus the rejection of these claims is also unsupported in the art for at least the above highlighted reasons. Each of claims 22-32 and 63-65 recite additional combinations of features not taught or suggested in the cited art.

Claim 33 recites a combination of features including: "generating a mode indication indicative of whether or not a first mode defined in a processor architecture is active, the generating responsive to the first indication and the second indication; and storing the mode indication in a third addressable storage location". While the specific teachings of Turley that are alleged to correspond to the above highlighted features are unclear (see the discussion above), Applicants can find no teaching in the cited section of Turley that teaches or suggests the above highlighted features.

For at least the above highlighted reasons, Applicants submit that rejection of claim 33 is unsupported in the art and should be withdrawn. Claims 34-43 depend from claim 33, and thus the rejection of these claims is also unsupported in the art for at least the above highlighted reasons. Each of claims 34-43 recite additional combinations of features not taught or suggested in the cited art.

Claims 44-49

Applicants respectfully submit that each of claims 44-49 recites a combination of features not taught or suggested in Turley. For example, claim 44 recites a combination of features including: "A carrier medium carrying a set of instructions for activating a first mode in a processor, the set of instructions including: a first one or more instructions to update a first indication to indicate that physical address extension is enabled; a second one or more instructions to update a page table base register to point to a set of page tables; a third one or more instructions to update an enable indication to an enabled state; and a fourth one or more instructions to update a paging indication to indicate that paging is enabled." While the specific teachings of Turley that are alleged to correspond to the

above highlighted features are unclear (see the discussion above), Applicants can find no teaching in the cited section of Turley of a carrier medium carrying any set of instructions. Furthermore, Turley does not teach or suggest a set of instructions comprising the first one or more instructions, the second one or more instructions, the third one or more instructions, and the fourth one or more instructions highlighted above.

For at least the above highlighted reasons, Applicants submit that rejection of claim 44 is unsupported in the art and should be withdrawn. Claims 45-47 depend from claim 44, and thus the rejection of these claims is also unsupported in the art for at least the above highlighted reasons. Each of claims 45-47 recite additional combinations of features not taught or suggested in the cited art.

Claim 48 recites a combination of features including: "A carrier medium carrying a set of instructions for deactivating a first mode in a processor, the set of instructions including: a first one or more instructions to update a paging indication to indicate that paging is disabled; a second one or more instructions to update a page table base register to point to a set of page tables; and a third one or more instructions to update an enable indication to a disabled state." While the specific teachings of Turley that are alleged to correspond to the above highlighted features are unclear (see the discussion above), Applicants can find no teaching in the cited section of Turley of a carrier medium carrying any set of instructions. Furthermore, Turley does not teach or suggest a set of instructions comprising the first one or more instructions, the second one or more instructions, and the third one or more instructions highlighted above.

For at least the above highlighted reasons, Applicants submit that rejection of claim 48 is unsupported in the art and should be withdrawn. Claim 49 depends from claim 48, and thus the rejection of this claim is also unsupported in the art for at least the above highlighted reasons. Claim 49 recites additional combinations of features not taught or suggested in the cited art.

New Claims

Applicants respectfully submit that each of new claims 50-71 recite combinations of features not taught or suggested in the cited art. For example, claim 50 recites a combination of features including: "the circuit is configured to generate a mode indication responsive to the enable indication and the paging indication, wherein the mode indication is indicative of whether or not a first mode of the processor is active, the first mode permitting an address size greater than 32 bits and an operand size greater than 32 bits, and wherein the circuit is configured to store the mode indication in a location addressable by an instruction". Claims 51-62 depend from claim 50, and recite additional combinations of features. Claims 63-65 depend from claim 21, as highlighted above. Claim 66 recites a combination of features including: "generate a mode indication responsive to the first indication and the second indication, the mode indication indicative of whether or not a first mode is active in a processor; and update a third storage location configured to store the mode indication". Claims 67-71 depend from claim 66 and recite additional combinations of features.

Information Disclosure Statements (IDSs)

Applicants received the signed and initialed PTO-1449 forms from the IDSs previously filed in the present application. However, the PTO-1449 form from the IDS mailed November 8, 2002 (and received in the PTO on November 13, 2002) is missing the Examiner's initials next to the reference B9. As the reference is not crossed out, Applicants presume this is merely an oversight. Applicants include a copy of the PTO-1449 form attached to this response, with the missing initials highlighted. Applicants respectfully request that the Examiner initial the attached PTO-1449 form and return it with the next Action. Additionally, Applicants file herewith another IDS.

CONCLUSION

Applicants submit that the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-66500/LJM.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☐ Petition for Extension of Time

☐ Notice of Change of Address

☒ Please debit the above deposit account in the amount of $748 for fees ($180 IDS fee, $172 for 2 excess independent claims, $396 for 22 excess claims over 20).

☒ Other: IDS, PTO-1449 form from previous IDS with missing initials highlighted

Respectfully submitted,

Lawrence J. Merkel
Reg. No. 41,191
AGENT FOR APPLICANT(S)

Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8800

Date: 9/7/04